Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (**canceled**)

2. (**currently amended**): The semiconductor device according to claim [[1]] 4, wherein the part that is vulnerable to soft errors is a first diffusion layer region, and the first diffusion layer region is at least a part of diffusion layer regions formed in the MOS type transistor structure and is connected to neither a power supply nor a ground.

3. (**canceled**)

4. (**currently amended**): ~~The~~ A semiconductor device ~~according to claim 3~~ having a metal oxide semiconductor (MOS) type transistor structure, comprising:

an additional load capacitance that is formed at a part of the semiconductor device, which is vulnerable to soft errors;

wherein the formation of the additional load capacitance is performed such that a first well region that is formed immediately below the first diffusion layer region is made to have a higher concentration than a second well region; and

wherein an impurity concentration at a junction interface between the first well region with the higher concentration and the first diffusion layer region is set at 5×10^{18} to $10^{19}/cm^3$, and an impurity concentration at a junction interface between the ~~other~~ second well region and a second diffusion layer region which is the diffusion layer regions except for the first diffusion layer region is set at $10^{18}/cm^3$.

5. (**withdrawn/currently amended**): The semiconductor device according to claim [[1]] 4, wherein the semiconductor device having the MOS type transistor structure includes at least an n-type MOS transistor, and

the part that is vulnerable to soft errors is a drain of the n-type MOS type transistor.

6. (**withdrawn**): The semiconductor device according to claim 5, wherein the semiconductor device having the MOS type transistor structure is a static random access memory (SRAM) type memory cell having a flip-flop circuit that comprises a plurality of the n-type MOS transistors and a plurality of p-type MOS transistors.

7. (**withdrawn/currently amended**): The semiconductor device according to claim [[1]] 4, wherein the semiconductor device having the MOS type transistor structure includes at least an n-type MOS transistor and a p-type MOS transistor, and

the part that is vulnerable to soft errors is a drain of the n-type MOS transistor and a drain of the p-type MOS transistor.

8. (**withdrawn**): The semiconductor device according to claim 7, wherein the semiconductor device having the MOS type transistor structure is a static random access memory (SPAM) type memory cell having a flip-flop circuit that comprises a plurality of the n-type MOS transistors and a plurality of the p-type MOS transistors.

9. – 20. (**canceled)**